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GREGORY D. CALDWELL
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025

EXAMINER
MILLS, DONALD L

ART UNIT	PAPER NUMBER
2662	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/585,744	MIAO, KAI	
	Examiner	Art Unit	
	Donald L Mills	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *27-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,15-20 and 22-26* is/are rejected.

7)☒ Claim(s) *14 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-26, drawn to communication parameters, classified in class 370, subclass 252.

II. Claims 27-29, drawn to synchronization, classified in class 370, subclass 503.

2. Inventions communication parameters and synchronization are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different modes of operation, different functions, or different effects (MPEP § 806.04, MPEP § 808.01). In the instant case the different inventions have different functions, communication parameters relates to transmitting packets based upon a calculated delay while synchronization relates to synchronizing the clock of a receiver.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Gregory D. Caldwell on September 16, 2003 a provisional election was made with traverse to prosecute the invention of communication parameters, claims 1-26. Affirmation of this election must be made by applicant in replying to this Office action. Claims 27-29 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference signs mentioned in the description: "t_n" (Page 9, line 14).

4. The drawings are objected to because:

Figure 3, "T_{ed}" should be corrected to "t_{ed}". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

5. The disclosure is objected to because of the following informalities:

Page 2, line 16, "Additionally,the" should be corrected to "Additionally, the".

Page 6, line 9, "at" should be corrected to "to".

Page 8, line 4, "401-403and" should be corrected to "401-403 and".

Page 12, line 21, "1004loads" should be corrected to "1004 loads".

The specification lacks a Brief Summary of the Invention section, which is separate and distinct from the abstract and directed toward the invention rather than the disclosure as a whole.

Appropriate correction is required.

Claim Objections

6. Claim 11 is objected to because of the following informalities:

Regarding claim 11, page 17, line 1, "comprising::" should be corrected to "comprising:". Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 11-13, 15, 22, 23, 25, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by De Prycker (US 4,817,085).

Regarding claim 11, De Prycker discloses a system, which comprises:

Receiving a packet (Referring to Figure 1, a packet is received by the destination interface circuit **NAI**. See column 3, lines 51-52.)

Reading information in the packet and ascertaining therefrom a delay incurred by the packet in traversing the network (Referring to Figure 1, the packets are read by **EM2.** Where the packets have a random delay, **t0**, **t1**, **tk**, ... based upon their path through the **PSN**. See column 3, lines 54-57.)

Delaying use of the packet to reconstruct an analog signal by a calculated amount of time sufficient to make the calculated amount of time plus the ascertained delay substantially equal to the optimal delay (Referring to Figures 1 and 2, the packet is delayed for reconstruction by a calculated delay **Tm** and random delay **to** equal to the delay time **Tr**. See column 4, lines 11-12 and column 6, lines 8-11.)

Regarding claim 12, De Prycker discloses *setting the optimal delay at an amount equal to a minimum delay required to cause a specified probability of packet loss* (Referring to Figures 1 and 2, **Tr** is set equal to **T2** or larger so that no packets will be lost. See column 6, lines 10-12.)

Regarding claim 13, De Prycker discloses *the required minimum delay is recalculated every Nth packet, where N is a positive integer* (Referring to Figures 1 and 2, the first packet **DP0** is submitted to a total delay **T2**. See column 4, lines 11-12.)

Regarding claim 15, De Prycker discloses a system, which comprises:

A CPU for calculating a delay to which each of a plurality of received packets should be subjected (Referring to Figure 1, the common computer **CC** controls the timing circuit **TC** for controlling the delay of the packets. See column 3, lines 9-11 and lines 64-66.)

A buffer for storing the received packets (Referring to Figure 1, buffer unit **BU** stores the received packets. See column 3, lines 60-61.)

A timer for subjecting each packet to a calculated delay (Referring to Figure 1, the timer circuit **TC** counts a time **Tm**. See column 3, lines 65-66,) *that equals an optimal delay minus a network delay experienced by the packet* (Referring to Figures 1 and 2, the first packet **DP0** is submitted to a total delay **T2**, that includes a random delay **t0**. The difference between the total delay and random delay is inherent in the mathematical equation **T2=to+Tm**. See column 3, line 56 and column 4, lines 12-13,) *unless such calculated delay exceeds a predetermined maximum, in which case the predetermined maximum is utilized as the calculated delay* (Referring to Figures 1 and 2, the buffer **BU** has been given a maximum size corresponding to a delay time **Tr** such that **Tr** remains larger than or equal to **T2**. See column 6, lines 9-11.)

Regarding claim 22, De Prycker discloses a system, which comprises:

A signal processor for calculating a delay experienced by each of a plurality of packets through a data network (Referring to Figure 1, the packets are read by **EM2.** Where the packets have a random delay, **t0**, **t1**, **tk**, ... based upon their path through the **PSN**. See column 3, lines 54-57.)

A buffer system for delaying further conveyance of each of the packets by an amount of time dependent upon (Referring to Figures 1 and 2, the buffer **BU** has been given a maximum size corresponding to a delay time **Tr**, which is equal to **T2**, so that the packets are delayed. See column 6, lines 9-11,) *(1) a probability distribution updated in response to receipt and processing of selected ones of each of the packets* (The probability density function is generated in response to the first packet **DP0**. See column 6, lines 30,) *and (2) the calculated delay* (Referring to Figure 1, **T2=to+Tm**, where **to** is the random delay through the network. See column 5, lines 59-67.)

Regarding claim 23, De Prycker discloses *the buffer system arranged to delay further conveyance by an amount also dependant upon a prestored maximum* (Referring to Figures 1 and 2, buffer unit **BU** can store packets for a longer time equal to **Tr** as a maximum size. See column 4, lines 14-16.)

Regarding claim 25, De Prycker discloses *an interrupt generator for generating an interrupt when the amount of time for each packet expires* (Referring to Figures 1 and 2, discarding is performed when a packet **DPK** does not arrive in time. See column 4, lines 65-67.)

Regarding claim 26, De Prycker discloses *a poller for sequentially polling each of a plurality of storage locations within the buffer system to determine if a packet within the storage location is to be further conveyed* (Referring to Figures 1 and 2, a packet search circuit **PSC**

searches in the buffer unit **BU** for the first packet **DP0** and transfers it to the depacketizer circuit **DPA** at the appropriate clock interval and then searches for the next packet, if the packet is not available it is discarded (See column 3, lines 66-68 and column 4, lines 1-8.)

9. Claims 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Lauret (US 2002/0191645A1).

Regarding claim 16, Lauret discloses a method, which comprises:

Receiving a first packet at a gateway (Referring to Figure 15, an ATM receiver receives ATM cells. See page 3, section 50, lines 2-3.)

Assuming a reasonable value of a delay the packet experienced in traversing a network (Referring to Figure 4, assume **D** is the difference between **SRTSreceived-SRTSlocal**, which is inherently the transmission delay between ATM cells through the network. See page 3, section 54, lines 1-2.)

Setting a clock at the receiving gateway to a value equal to a time stamp contained within the first packet plus the reasonable value (Referring to Figure 4, the clock frequency at the ATM receiver is set according to **SRTSreceived** and **D**. See page 3, section 54, lines 1-7.)

Regarding claim 17, Lauret discloses *receiving packets in addition to the first packet, reading a time stamp from the additional packets* (Referring to Figure 4, received ATM cells SRTSs are extracted. See page 3, section 51, lines 4-6,) *calculating network delay for each of the additional packets based upon the clock at the receiving gateway and the timestamp from each of the additional packets* (Referring to Figure 4, assume **D** is the difference between **SRTSreceived-SRTSlocal**, which is inherently the transmission delay between ATM cells through the network. See page 3, section 54, lines 1-2.)

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-10 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over De Prycker (US 4,817,085).

Regarding claims 1-4, De Prycker discloses a system, which comprises a *storage location for storing packets received from a network* (Referring to Figure 1, buffer unit **BU**, exchange memory **EM2**, and package recognition circuit **PRC** store packets received from the PSN. See column 3, lines 7-9.) *A system for dynamically calculating a probability distribution associated with network delays for plural packets* (The system calculates the probability density function based upon the delay required for proper transmission through the network for the packets. See column 6, line30.) And, a *CPU for calculating, based upon the dynamically calculated probability distribution, a delay associated with the storage location,* (The computer **CC** controls the distribution, which inherently includes the calculation of the probability density function and the buffer delay associated with the packet. See column 3, lines 65-67 and column 4, lines 11-15,) *and for causing a packet in the storage location to be transmitted out of the storage location after an amount of time equal to the delay associated with the storage location* (The packets are transmitted from the **BU** and **PRC** according to the total delay suffered by the

packet which is dependent on buffer delay. See column 3, lines 65-67 and column 4, lines 11-15.)

De Prycker further discloses a system wherein *the CPU calculates a difference between the optimal delay permissible to guarantee a predetermined probability of packet loss, and an actual delay experienced by the packet for which the calculation is being done (Claim 2)* (Referring to Figures 1 and 2, the first packet **DP0** is submitted to a total delay **T2**, which guarantees a predetermined probability of loss, that includes a random delay **t0**. The difference between the total delay and random delay is inherent in the mathematical equation **T2=to+Tm**. See column 3, line 56 and column 4, lines 12-13.) And, *the probability distribution is updated every Nth packet received, where N is a positive integer (Claim 3)/where N is 1 (Claim 4)* (Referring to Figures 1 and 2, the probability distribution calculation includes packets **DP0, DP1, DPk**. See column 4, lines 33-45.)

De Prycker does not disclose *a plurality of storage locations.*

De Prycker teaches a system where the delay is calculated based upon a predetermined probability that the errors in the delayed packets, which are stored in a buffer, are always less than a predetermined value (See column 2, lines 3-6.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize multiple buffers. One of ordinary skill in the art at the time the invention was made would have been motivated to do so because unexpected results would not have been produced.

Regarding claims 5-8, De Prycker discloses: *an analog to digital (A/D) converter, the A/D converter being connected to the buffer* (The user circuit **UC** generates and receives a

continuous bit-stream of voice, video or other data; which, inherently includes an A/D converter and storage means in order to digitize the traffic for communication across the network. See column 3, lines 16-19.) *A Central Processing Unit (CPU) for causing packets arriving from a network at the apparatus to be stored in the buffer* (Referring to Figure 1, the common computer CC controls the storage of packets in buffer unit **BU**. See column 3, lines 59-61,) *the CPU also being arranged to calculate, upon receipt of every Nth packet or data, an optimal delay beyond which a packet will be lost* (When the whole packet **DPk** does not arrive in time it is discarded. See column 4, lines 65-66.) And, *a timer for causing each packet to incur an added delay* (The timer circuit **TC** counts a time **Tm**. See column 3, lines 65-66,) *at the gateway of the difference between the calculated optimal delay and the actual delay experienced by each packet* (Referring to Figures 1 and 2, the first packet **DP0** is submitted to a total delay **T2**, which guarantees a predetermined probability of loss, that includes a random delay **to**. The difference between the total delay and random delay is inherent in the mathematical equation **T2=to+Tm**. See column 3, line 56 and column 4, lines 12-13.)

De Prycker further discloses *wherein N is greater than 1 (Claim 6)/wherein N is 1 (Claim 7)* (Referring to Figures 1 and 2, the probability distribution calculation includes packets **DP0, DP1, DPk**. See column 4, lines 33-45.) And, *a network interface card for receiving signals from the data network (Claim 8)* (Referring to Figure 1, the sender/receiver circuit **SEND/REC** is coupled to the packet switching network **PSN**. See column 2, lines 61-64.)

De Prycker does not disclose *plural buffers*.

De Prycker teaches a system where the delay is calculated based upon a predetermined probability that the errors in the delayed packets, which are stored in a buffer, are always less than a predetermined value (See column 2, lines 3-6.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize multiple buffers. One of ordinary skill in the art at the time the invention was made would have been motivated to do so because unexpected results would not have been produced.

Regarding claim 9 as explained above in the rejection statement of claim 5, De Prycker discloses all the claim limitations of claim 5 (parent claim). De Prycker does not disclose *the CPU as a Digital Signal Processing (DSP) chip that performs DSP and control functions.*

De Prycker teaches a user circuit that generates and receives a continuous bit-stream, which may be constituted by voice, video, or other data or a mixture thereof; which, inherently includes an A/D converter in order to digitize the traffic for communication across the network (See column 3, lines 16-19.) De Prycker further teaches a common computer **CC,** which controls the system (See column 3, lines 3-6.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the functions of the user circuit and common computer into one processor. One of ordinary skill in the art at the time the invention was made would have been motivated to do so because unexpected results would not have been produced.

Regarding claim 10 as explained above in the rejection statement of claim 5, De Prycker discloses all the claim limitations of claim 5 (parent claim). De Prycker does not disclose the *network interface card as implementing the G.723 or G.729 standard.*

De Prycker teaches a sender/receiver circuit **SEND/REC** that is coupled to the packet switching network **PSN** (See column 2, lines 61-64.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the G.723 or G.729 standard in the sender/receiver circuit. One of ordinary skill in the art at the time the invention was made would have been motivated to do so because the G.723 and G.729 standards are well known in the art.

Regarding claim 24 as explained above in the rejection statement of claim 22, De Prycker discloses all the claim limitations of claim 22 (parent claim). De Prycker does not disclose the *signal processor as programmed to use a recursive algorithm.*

De Prycker teaches a system where the delay is calculated based upon a predetermined probability that the errors in the delayed packets are always less than a predetermined value, which is based upon network delay (See column 2, lines 3-6.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the calculation of network delay in a recursive algorithm. One of ordinary skill in the art at the time the invention was made would have been motivated to do so because recursive algorithms are well known in the art.

12. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lauret (US 2002/0191645A1) in view of De Prycker (US 4,817,085).

Regarding claim 18 as explained above in the rejection statement of claim 16, Lauret discloses all the claim limitations of claim 16 (parent claim). Lauret does not disclose *updating a probability distribution function of network delays after receipt of every Nth packet, where N is a positive integer.*

De Prycker teaches a system where the delay is calculated based upon a predetermined probability that the errors in the delayed packets are always less than a predetermined value, which is based upon network delay (See column 2, lines 3-6.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the digital clock recovery method of Lauret in the data communication packet switch of De Prycker, which supports a continuous bit stream of voice, video, or data (See column 1, lines 58-60.) One of ordinary skill in the art at the time the invention was made would have been motivated to do so in order to recover the clock frequency of a constant bit stream (See Lauret, page 1, section 2, lines 12-14.)

Regarding claim 19 as explained above in the rejection statement of claim 18, Lauret and De Prycker disclose all the claim limitations of claim 18. Lauret and De Prycker do not disclose *updating using a recursive algorithm.*

De Prycker teaches a system where the delay is calculated based upon a predetermined probability that the errors in the delayed packets are always less than a predetermined value, which is based upon network delay (See column 2, lines 3-6.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the calculation of network delay in a recursive algorithm. One of ordinary skill in the art at the time the invention was made would have been motivated to do so because recursive algorithms are well known in the art.

13. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lauret (US 2002/0191645A1) in view of De Prycker (US 4,817,085) in further view of Agrawal et al. (US 5,623,483), hereinafter referred to as Agrawal.

Regarding claim 20 as explained above in the rejection statement of claim 16, Lauret and De Prycker disclose all the claim limitations of claim 16 (parent claim). Lauret and De Prycker do not disclose *updating comprising recalculating a buffer latency.*

Agrawal teaches a synchronization system for networked multimedia streams which calculates the buffer delay for a packet based upon its pointer in a point list (See column 4, lines 19-22.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the buffer delay counter of Agrawal in the data communications system of De Prycker. One of ordinary skill in the art at the time the invention was made would have been motivated to do so in order to track the delay of packets or cells in the buffer.

Allowable Subject Matter

14. Claims 14 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donald L Mills whose telephone number is 703-305-7869. The examiner can normally be reached on 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 703-305-4744. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4700.

Donald L Mills

September 16, 2003

CHAU NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600